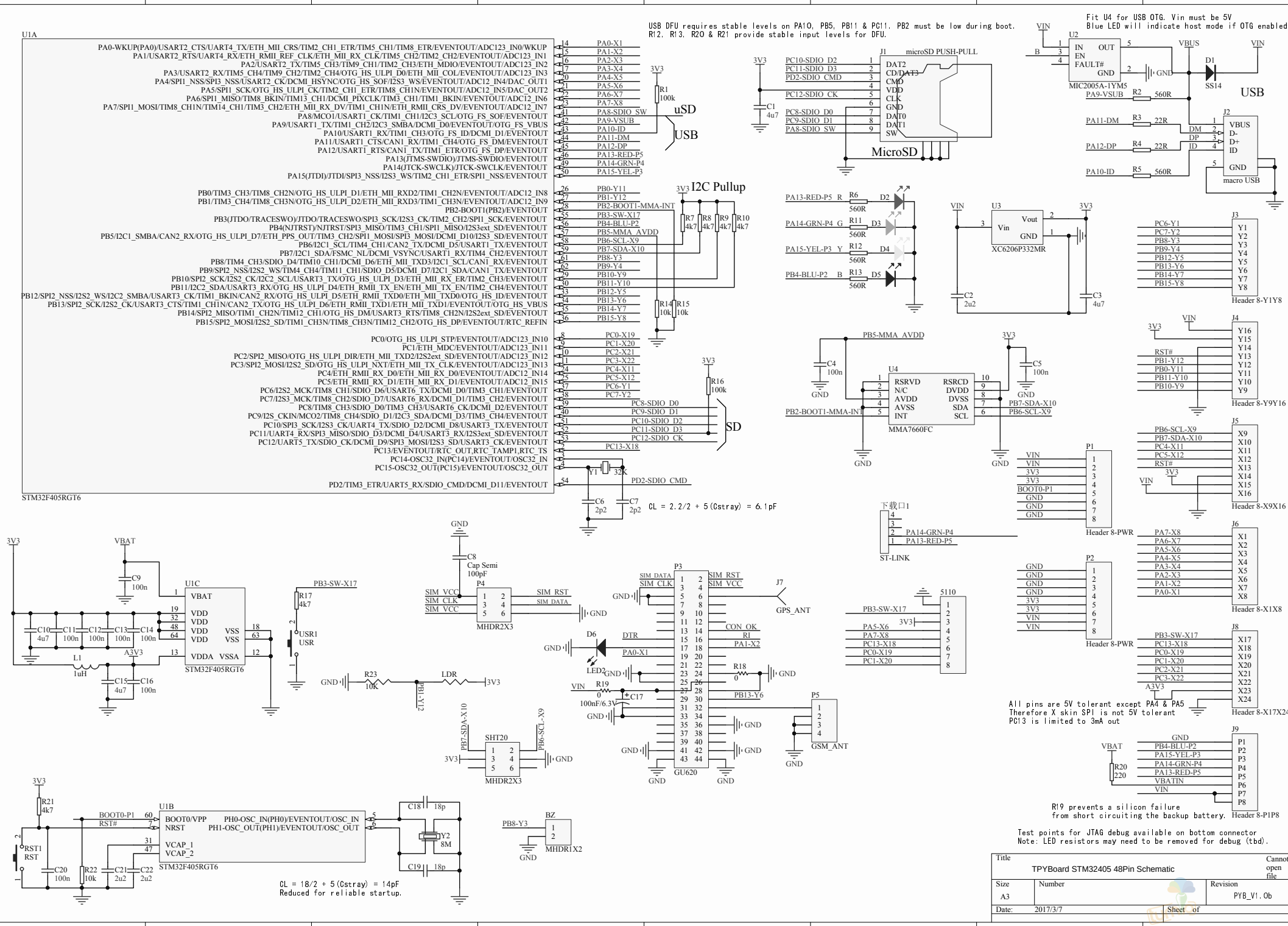
USB DFU requires stable levels on PA10, PB5, PB11 & PC11. PB2 must be low during boot.
R12, R13, R20 & R21 provide stable input levels for DFU.
Fit U4 for USB OTG. Vin must be 5V
Blue LED will indicate host mode if OTG enabled.
U1A
PA0-WKUP(PA0)/USART2_CTS/UART4_TX/ETH_MII_CRS/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR/EVENTOUT/ADC123_IN0/WKUP
PA1/USART2_RTS/UART4_RX/ETH_RMII_REF_CLK/ETH_MII_RX_CLK/TIM5_CH2/TIM2_CH2/EVENTOUT/ADC123_IN1
PA2/USART2_TX/TIM5_CH3/TIM9_CH1/TIM2_CH3/ETH_MDIO/EVENTOUT/ADC123_IN2
PA3/USART2_RX/TIM5_CH4/TIM9_CH2/TIM2_CH4/OTG_HS_ULPI_D0/ETH_MII_COL/EVENTOUT/ADC123_IN3
PA4/SPI1_NSS/SPI3_NSS/USART2_CK/DCMI_HSYNC/OTG_HS_SOF/I2S3_WS/EVENTOUT/ADC12_IN4/DAC_OUT1
PA5/SPI1_SCK/OTG_HS_ULPI_CK/TIM2_CH1_ETR/TIM8_CH1N/EVENTOUT/ADC12_IN5/DAC_OUT2
PA6/SPI1_MISO/TIM8_BKIN/TIM13_CH1/DCMI_PIXCLK/TIM3_CH1/TIM1_BKIN/EVENTOUT/ADC12_IN6
PA7/SPI1_MOSI/TIM8_CH1N/TIM14_CH1/TIM3_CH2/ETH_MII_RX_DV/TIM1_CH1N/ETH_RMII_CRS_DV/EVENTOUT/ADC12_IN7
PA8/MCO1/USART1_CK/TIM1_CH1/I2C3_SCL/OTG_FS_SOF/EVENTOUT
PA9/USART1_TX/TIM1_CH2/I2C3_SMBA/DCMI_D0/EVENTOUT/OTG_FS_VBUS
PA10/USART1_RX/TIM1_CH3/OTG_FS_ID/DCMI_D1/EVENTOUT
PA11/USART1_CTS/CAN1_RX/TIM1_CH4/OTG_FS_DM/EVENTOUT
PA12/USART1_RTS/CAN1_TX/TIM1_ETR/OTG_FS_DP/EVENTOUT
PA13(JTMS-SWDIO)/JTMS-SWDIO/EVENTOUT
PA14(JTCK-SWCLK)/JTCK-SWCLK/EVENTOUT
PA15(JTDI)/JTDI/SPI3_NSS/I2S3_WS/TIM2_CH1_ETR/SPI1_NSS/EVENTOUT
PB0/TIM3_CH3/TIM8_CH2N/OTG_HS_ULPI_D1/ETH_MII_RXD2/TIM1_CH2N/EVENTOUT/ADC12_IN8
PB1/TIM3_CH4/TIM8_CH3N/OTG_HS_ULPI_D2/ETH_MII_RXD3/TIM1_CH3N/EVENTOUT/ADC12_IN9
PB2-BOOT1(PB2)/EVENTOUT
PB3(JTDO/TRACESWO)/JTDO/TRACESWO/SPI3_SCK/I2S3_CK/TIM2_CH2/SPI1_SCK/EVENTOUT
PB4(NJTRST)/NJTRST/SPI3_MISO/TIM3_CH1/SPI1_MISO/I2S3ext_SD/EVENTOUT
PB5/I2C1_SMBA/CAN2_RX/OTG_HS_ULPI_D7/ETH_PPS_OUT/TIM3_CH2/SPI1_MOSI/SPI3_MOSI/DCMI_D10/I2S3_SD/EVENTOUT
PB6/I2C1_SCL/TIM4_CH1/CAN2_TX/DCMI_D5/USART1_TX/EVENTOUT
PB7/I2C1_SDA/FSMC_NL/DCMI_VSYNC/USART1_RX/TIM4_CH2/EVENTOUT
PB8/TIM4_CH3/SDIO_D4/TIM10_CH1/DCMI_D6/ETH_MII_TXD3/I2C1_SCL/CAN1_RX/EVENTOUT
PB9/SPI2_NSS/I2S2_WS/TIM4_CH4/TIM11_CH1/SDIO_D5/DCMI_D7/I2C1_SDA/CAN1_TX/EVENTOUT
PB10/SPI2_SCK/I2S2_CK/I2C2_SCL/USART3_TX/OTG_HS_ULPI_D3/ETH_MII_RX_ER/TIM2_CH3/EVENTOUT
PB11/I2C2_SDA/USART3_RX/OTG_HS_ULPI_D4/ETH_RMII_TX_EN/ETH_MII_TX_EN/TIM2_CH4/EVENTOUT
PB12/SPI2_NSS/I2S2_WS/I2C2_SMBA/USART3_CK/TIM1_BKIN/CAN2_RX/OTG_HS_ULPI_D5/ETH_RMII_TXD0/ETH_MII_TXD0/OTG_HS_ID/EVENTOUT
PB13/SPI2_SCK/I2S2_CK/USART3_CTS/TIM1_CH1N/CAN2_TX/OTG_HS_ULPI_D6/ETH_RMII_TXD1/ETH_MII_TXD1/EVENTOUT/OTG_HS_VBUS
PB14/SPI2_MISO/TIM1_CH2N/TIM12_CH1/OTG_HS_DM/USART3_RTS/TIM8_CH2N/I2S2ext_SD/EVENTOUT
PB15/SPI2_MOSI/I2S2_SD/TIM1_CH3N/TIM8_CH3N/TIM12_CH2/OTG_HS_DP/EVENTOUT/RTC_REFIN
PC0/OTG_HS_ULPI_STP/EVENTOUT/ADC123_IN10
PC1/ETH_MDC/EVENTOUT/ADC123_IN11
PC2/SPI2_MISO/OTG_HS_ULPI_DIR/ETH_MII_TXD2/I2S2ext_SD/EVENTOUT/ADC123_IN12
PC3/SPI2_MOSI/I2S2_SD/OTG_HS_ULPI_NXT/ETH_MII_TX_CLK/EVENTOUT/ADC123_IN13
PC4/ETH_RMII_RX_D0/ETH_MII_RX_D0/EVENTOUT/ADC12_IN14
PC5/ETH_RMII_RX_D1/ETH_MII_RX_D1/EVENTOUT/ADC12_IN15
PC6/I2S2_MCK/TIM8_CH1/SDIO_D6/USART6_TX/DCMI_D0/TIM3_CH1/EVENTOUT
PC7/I2S3_MCK/TIM8_CH2/SDIO_D7/USART6_RX/DCMI_D1/TIM3_CH2/EVENTOUT
PC8/TIM8_CH3/SDIO_D0/TIM3_CH3/USART6_CK/DCMI_D2/EVENTOUT
PC9/I2S_CKIN/MCO2/TIM8_CH4/SDIO_D1/I2C3_SDA/DCMI_D3/TIM3_CH4/EVENTOUT
PC10/SPI3_SCK/I2S3_CK/UART4_TX/SDIO_D2/DCMI_D8/USART3_TX/EVENTOUT
PC11/UART4_RX/SPI3_MISO/SDIO_D3/DCMI_D4/USART3_RX/I2S3ext_SD/EVENTOUT
PC12/UART5_TX/SDIO_CK/DCMI_D9/SPI3_MOSI/I2S3_SD/USART3_CK/EVENTOUT
PC13/EVENTOUT/RTC_OUT,RTC_TAMP1,RTC_TS
PC14-OSC32_IN(PC14)/EVENTOUT/OSC32_IN
PC15-OSC32_OUT(PC15)/EVENTOUT/OSC32_OUT
PD2/TIM3_ETR/UART5_RX/SDIO_CMD/DCMI_D11/EVENTOUT
STM32F405RGT6
PA0-X1
PA1-X2
PA2-X3
PA3-X4
PA4-X5
PA5-X6
PA6-X7
PA7-X8
PA8-SDIO_SW
PA9-VSUB
PA10-ID
PA11-DM
PA12-DP
PA13-RED-P5
PA14-GRN-P4
PA15-YEL-P3
PB0-Y11
PB1-Y12
PB2-BOOT1-MMA-INT
PB3-SW-X17
PB4-BLU-P2
PB5-MMA_AVDD
PB6-SCL-X9
PB7-SDA-X10
PB8-Y3
PB9-Y4
PB10-Y9
PB11-Y10
PB12-Y5
PB13-Y6
PB14-Y7
PB15-Y8
PC0-X19
PC1-X20
PC2-X21
PC3-X22
PC4-X11
PC5-X12
PC6-Y1
PC7-Y2
PC8-SDIO_D0
PC9-SDIO_D1
PC10-SDIO_D2
PC11-SDIO_D3
PC12-SDIO_CK
PC13-X18
PD2-SDIO_CMD
3V3
R1 100k
uSD
USB
I2C Pullup
R7 4k7
R8 4k7
R9 4k7
R10 4k7
R14 10k
R15 10k
R16 100k
SD
Y1 32K
C6 2p2
C7 2p2
CL = 2.2/2 + 5(Cstray) = 6.1pF
J1 microSD PUSH-PULL
DAT2
CD/DAT3
CMD
VDD
CLK
GND
DAT0
DAT1
SW
C1 4u7
MicroSD
U2
IN
OUT
EN
FAULT#
GND
MIC2005A-1YM5
VBUS
D1
SS14
USB
R2 560R
J2
VBUS
D-
D+
ID
GND
macro USB
R3 22R
R4 22R
R5 560R
R6 560R
R11 560R
R12 560R
R13 560R
D2
D3
D4
D5
U3
Vout
Vin
GND
XC6206P332MR
C2 2u2
C3 4u7
J3
Header 8-Y1Y8
J4
Header 8-Y9Y16
J5
Header 8-X9X16
J6
Header 8-X1X8
J8
Header 8-X17X24
J9
Header 8-P1P8
C4 100n
C5 100n
U4
RSRVD
N/C
AVDD
AVSS
INT
RSRCD
DVDD
DVSS
SDA
SCL
MMA7660FC
P1
P2
Header 8-PWR
下载口1
ST-LINK
5110
U1C
VBAT
VDD
VSS
VDDA
STM32F405RGT6
C8 Cap Semi 100pF
P4
MHDR2X3
P3
GU620
J7
GPS_ANT
P5
GSM_ANT
D6
LED2
R17 4k7
USR1
USR
R18 0
R19 0
C17 100nF/6.3V
R23 10k
LDR
SHT20
U1B
BOOT0/VPP
NRST
PH0-OSC_IN(PH0)/EVENTOUT/OSC_IN
PH1-OSC_OUT(PH1)/EVENTOUT/OSC_OUT
VCAP_1
VCAP_2
STM32F405RGT6
R21 4k7
RST1
RST
R22 10k
C18 18p
C19 18p
Y2 8M
CL = 18/2 + 5(Cstray) = 14pF
Reduced for reliable startup.
BZ
MHDR1X2
All pins are 5V tolerant except PA4 & PA5
Therefore X skin SPI is not 5V tolerant
PC13 is limited to 3mA out
R20 220
R19 prevents a silicon failure
from short circuiting the backup battery.
Test points for JTAG debug available on bottom connector
Note: LED resistors may need to be removed for debug (tbd).
Title
TPYBoard STM32405 48Pin Schematic
Cannot open file
Size
A3
Number
Revision
PYB_V1.0b
Date:
2017/3/7
Sheet of